CPE 2211 COMPUTER ENGINEERING LAB

EXPERIMENT 4 LAB MANUAL

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SSI COMBINATIONAL LOGIC DESIGN: A MULTI-FUNCTION GATE

OBJECTIVES

In this experiment you will

- Design, build, and document a Multi-Function Gate.
- Gain experience with use of Karnaugh Maps.
- Use the suite of EDA tools supplied by Altera: Quartus-II and ModelSim.

LAB REPORTS

The format of lab reports should be such that the information can be used to reproduce the lab, including what values were used in a circuit, why the values were used, how the values were determined, and any results and observations made. This lab manual will be used as a guide for what calculations need to be made, what values need to be recorded, and various other questions. The lab report does not need to repeat everything from the manual verbatim, but it does need to include enough information for a 3rd party to be able to use the report to obtain the same observations and answers. Throughout the lab manual, in the Preliminary (if there is one), and in the Procedure, there are areas designated by **Qxx followed by a question or statement**. These areas will be **bold**, and the lab TA will be looking for an answer or image for each. These answers or images are to be included in the lab report. The lab TA will let you know if the lab report will be paper form, or if you will be able to submit electronically.

PURPOSE

The purpose of this exercise is to design, build, and document a Multi-Function Gate using small scale integration (SSI) components from a verbal description.

REFERENCES

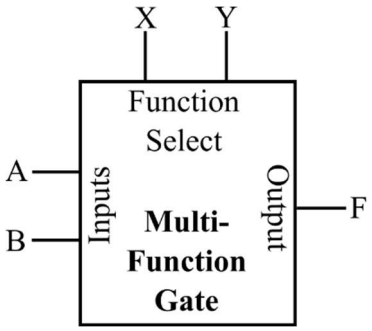
CpE112 Laboratory Manual: Appendix B and C, and Givone: Sections 4.4 – 4.6

MATERIALS REQUIRED

Assorted SSI components (see Appendix C), Breadboard

BACKGROUND

The Multi-Function Gate, shown in the block diagram of Figure 1, can perform four different logical operations of the data inputs, A and B, controlled by the operation select inputs, X and Y, as shown in the function table of Figure 1. The specific logic function for each X, Y input pair will be given to you by your instructor.



X	Y	Function
0	0	$F_0(A, B)$
0	1	$F_1(A, B)$
1	0	$F_2(A, B)$
1	1	$F_3(A, B)$

Figure 1: Block Diagram and Function Table for Multi-Function Gate.

PRELIMINARY

1. Represent the output F, as a function of A, B, X, and Y in a truth table.
2. Write the minimal 2-level logic expressions for F using either a sum-of-products (SOP) or a product of-sums (POS).
3. Draw a logic diagram for your SOP or POS expression.
4. Draw a complete schematic diagram of the Multi-Function Gate in Quartus II, using as few SSI components and as few levels of logic as possible. The format for a schematic diagram is similar as shown in Appendix B, but with slightly difference.
5. Simulate your design using ModelSim. Print out the logic diagram, and the waveforms for all possible input combinations.

PROCEDURE

1. Build your design from 4) in the Preliminary using SSI components.
2. Test all input combinations for your design to verify that it behaves exactly as desired by using dip switches for the inputs and LEDs for the output.

Q1. Can invert be assigned as one of the functions of the Multi-Function Gate? If yes, explain how.

Q2. Will a change in the number of outputs or data inputs affect the number of operation select lines? Explain.

Q3. Will a change in the number of functions affect the operation select lines? Explain.

Q4. How many unit loads does each input of your circuit present to gates that may drive them? One unit load is associated with each gate that must be directly driven by an input line. For example, the circuit in Appendix B has 3 unit loads for A, 3 for B, 3 for X, and 4 for Y.